AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

a plurality of transistors comprising different gate insulator film in their thickness value, said plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise ~~a first~~ lightly doped drain regions, ~~and~~

wherein said gate electrode includes an impurity to suppress depletion which is implanted when forming ~~a source region and a drain region~~ said lightly doped drain regions, and ~~one of said source region and said drain region is thinner than the other region~~

wherein said lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

2. (Previously Amended) The semiconductor device according to claim 1, wherein said plurality of transistors comprise a plurality of MOSFETs formed on a substrate.

3. (Previously Amended) The semiconductor according to claim 2,

wherein said MOSFET includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate insulator film than that of said I/O-purpose MOSFET and also has a smaller thickness of said gate electrode than that of said I/O-purpose MOSFET.

4-6 (Canceled)

7. (Currently Amended) The semiconductor device according to claim 1, wherein said plurality of transistors comprise a first lightly doped drain region and a second lightly doped drain region.

8. (Previously Added) The semiconductor device according to claim 7, wherein said first lightly doped drain region is deeper than said second lightly doped drain region.

9. (Currently Amended) The semiconductor device according to claim 3, wherein said I/O-purpose MOSFET comprises ~~said~~ a first lightly doped drain region.

10. (Currently Amended) The semiconductor device according to claim 3, wherein said core-purpose MOSFET comprises a ~~second~~ lightly doped drain region.

11. (Previously Added) The semiconductor device according to claim 2,

wherein said MOSFET includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate insulator film than that of said I/O-purpose MOSFET.

12. (Previously Added) The semiconductor device according to claim 2,

wherein said MOSFET includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate electrode than that of said I/O-purpose MOSFET.

13. (Previously Added) The semiconductor device according to claim 3, wherein said core-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 1.0v.

14. (Previously Added) The semiconductor device according to claim 3, wherein said I/O-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 3.3v.

15. (Previously Added) The semiconductor device according to claim 1, wherein said first lightly doped drain region comprises an I/O-purpose P-well with an N - type impurity at a predetermined density and a predetermined energy level, said N - type impurity comprises phosphorous.

16. (Previously Added) The semiconductor device according to claim 15,

wherein said predetermined density is about $2 \times 10^{13}/cm^2$, and

wherein said predetermined energy level is about 30 keV.

17. (Currently Amended) The semiconductor device according to claim ~~1~~7, wherein said second lightly doped drain region comprises a core-purpose P-well with an N - type impurity implanted at a predetermined density and a predetermined energy level used for implantation, said N - type impurity comprises arsenic.

18. (Previously Added) The semiconductor device according to claim 17,

wherein said predetermined density is about 5 x $10^{14}/cm^2$, and

wherein said predetermined energy level is about 2.5 keV.

19. (Previously Added) The semiconductor device according to claim 1,

wherein said plurality of transistors comprise a plurality of sidewalls, said plurality of sidewalls comprising a first sidewall and a second sidewall, and

wherein said first sidewall has a height greater than that of said second sidewall.

20. (Currently Amended) The semiconductor device according to claim 1, wherein said plurality of transistors comprise said ~~source region and said drain region~~ lightly doped drain regions with an N - type impurity implanted at a predetermined density and a predetermined energy level used for implantation, said N - type impurity comprises arsenic.

21. (Previously added) The semiconductor device according to claim 20,

wherein said predetermined density is about 5 x $10^{15}/cm^2$, and

wherein said predetermined energy level is about 30 keV.

22. (Currently Amended) A semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values, said plurality of types of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise a plurality of sidewalls, a first lightly doped drain region, and a second lightly doped drain region, where said first lightly doped drain region and said second lightly doped drain region are formed using said plurality of sidewalls and said gate electrode as a mask, and

wherein said first and second lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

23. (Currently Amended) A semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values with a polysilicon film layer, said plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said thickness of said gate insulator film varies based on the amount of deposited gate electrode materials,

wherein said plurality of transistors comprise a plurality of sidewalls, and lightly doped drain regions formed using said plurality of sidewalls and said gate electrode as a mask, and

wherein said lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.